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Novel Trench Gate Structure Developments Set the Benchmark for Next Generation Power MOSFET Switching Performance.

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ABSTRACT

As power system engineers from all market segments strive for more efficient power supply designs, demand is placed upon power MOSFET suppliers to improve the performance of the devices. This paper presents a new power Trench W-gated MOSFET (WMOSFET) structure that produces a quantum reduction in gate-drain miller capacitance C_{rss} without significantly degrading the $r_{DS(on)}$ of the MOSFET. An initial 35-V n-channel device, designed to have a 13-mΩ on resistance, was compared with a traditional gate structure MOSFET. The new W-gate MOSFET exhibited a 33% reduction in C_{rss} and a 50% reduction in the gate drain charge (Q_{gd}). The corresponding figure of merit ($r_{DS(on)}.Q_g$) reduction, compared with the conventional gate Trench MOSFET, showed a 60% improvement for the W-gate MOSFET.

SILICON STRUCTURE

Traditional Trench MOSFET gate structure.

The trench gated U-groove MOSFET or UMOSFET, has become the main structure when striving for ultra low $r_{DS(on)}$ performance in vertical trench power MOSFETs. However, conventional UMOSFETs (shown in Figure 1) suffer from an inherent high gate-drain capacitance especially when attempting to increase the cell density of the device. To further scale the size of the UMOSFET cell to reduce the $r_{DS(on)}$ value would degrade the switching performance significantly. Therefore the main objective for improving power MOSFET technologies is to increase cell density, without imposing high gate drain capacitance onto the MOSFET structure. One solution was proposed by Blanchard et al[1], who suggested a thicker gate oxide along the Trench wall, as shown in Figure 2. However, this type of structure does not provide the potential optimum performance of minimum C_{rss} since a certain overlap between the thin gate oxide and drain region is required to allow current flow. This overlap needs to take into consideration process variations in both trench and p-body junction depths and as such this makes it more difficult to manufacture a repeatable and accurate MOSFET structure.

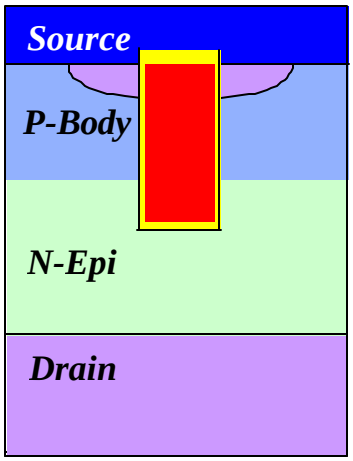

Figure 1. Schematic cross section of a conventional Trench MOSFET.

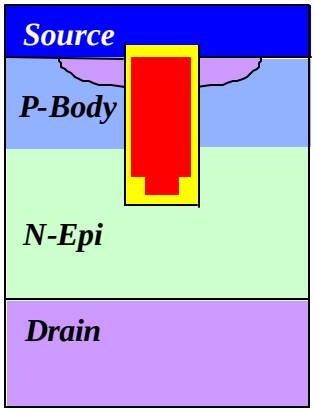

Figure 2. Schematic cross section of Trench MOSFET with thick bottom oxide.

Another method of reducing C_{rss} is to reduce the trench width to deep submicron dimensions[2]. However, this results in a lower current due to the pinch off effect of the inherent p-body JFET and as such is not a viable solution.

The W-gated Trench MOSFET

The improvement over state of the art structures is achieved by shaping the gate such that the thin oxide along the trench walls extends to the trench corners followed by a gradual transition to a thicker gate oxide at the bottom of the trench, which results in a W- shaped gate. The thick bottom oxide is self-aligned to the p-body / n-epi junction. Such improvement allows further increases in cell density, to enable lower specific $r_{DS(on)}$, without sacrificing switching performance due to the related increase in capacitance

The new proposed structure[3] is shown, in Figure 3, with the p-body/n-epi junction that is self-aligned to the transition between the thin and thicker gate oxide layer at the bottom of the trench. This is achieved with a lightly doped arsenic implant at the bottom of the trench, which minimises the impact of the thicker oxide on the $r_{DS(on)}$ and provides a good process margin. This therefore makes it possible to manufacture a repeatable and accurate device structure. Simulations show that this effect is further aided by:

1) a slower lateral than vertical diffusion of the p-body region
2) p-body boron segregation
3) n-epi phosphorus pile-up at the oxide interface.

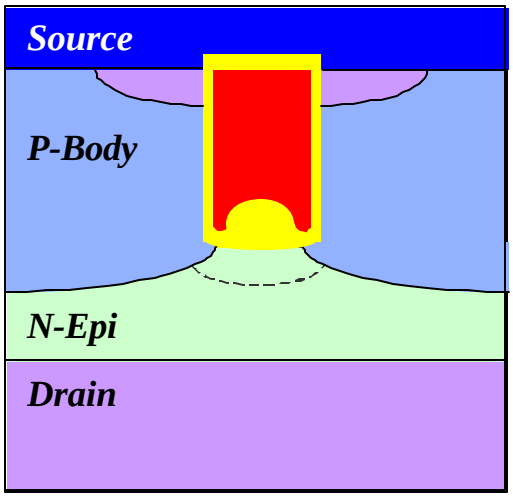

Figure 3. Schematic cross section of a W-gated Trench MOSFET (WMOSFET)

Initial devices have been fabricated using the PWM optimised 113M Cell/in^2 Trench MOSFET[4] process with the addition of a deposited nitride layer after trench etch and pad oxide growth. The nitride layer is then removed only from the trench bottom and a thick bottom oxide layer is then realised by either a LOCOS or SACVD processes. The LOCOS grown oxide provided high quality oxide, and stresses at the trench corners were minimised such that device reliability was not compromised. The alternative SACVD process utilises the high selectivity deposition rate of ozone-activated TEOS Sub-Atmospheric CVD on the exposed n-epi layer at the bottom of the trench using the nitride film as a mask on the trench sidewalls.

SIMULATION RESULTS

Figure 4 shows the simulation results of a UMOSFET against a WMOSFET, in the on state. As can be seen the current spread at the bottom of the trench does not suffer from a significant JFET pinching effect. However, a slight increase in on-resistance is predicted due to a higher resistance of the accumulation layer at the trench bottom. SEM cross-sections of fabricated W-gated Trench MOSFETs (WMOSFETs) are shown in Figure 5 and 6 with a thin oxide of 50nm and a thick bottom oxide of

150 nm. The devices were compared to conventional Trench MOSFETs fabricated using the same layout and core process.

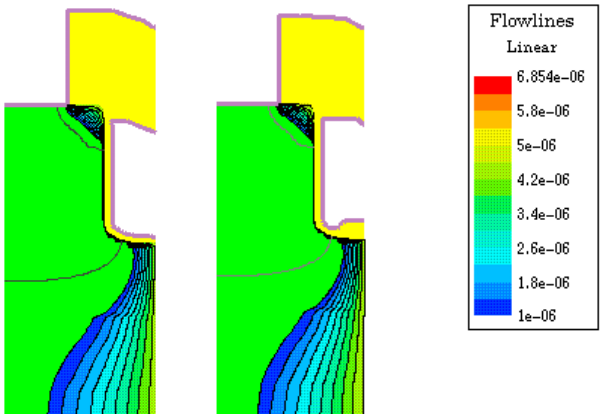

Figure 4. Current flow lines for Vgs=5Vin a) Conventional Trench MOSFET and b) W-gated Trench MOSFET (WMOSFET).

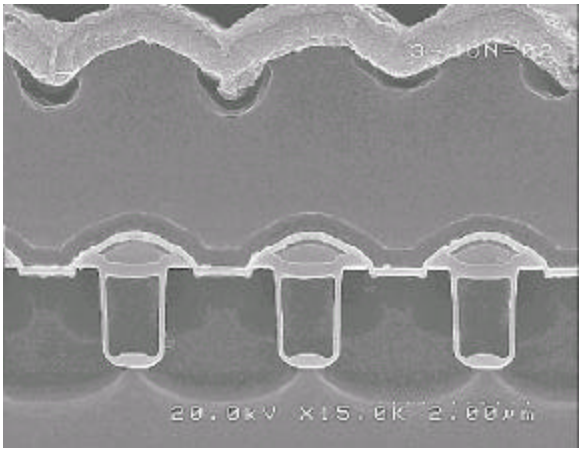

Figure 5. SEM cross-section of a W-gated Trench MOSFET multi-cell showing top metal and inter-layer dielectric.

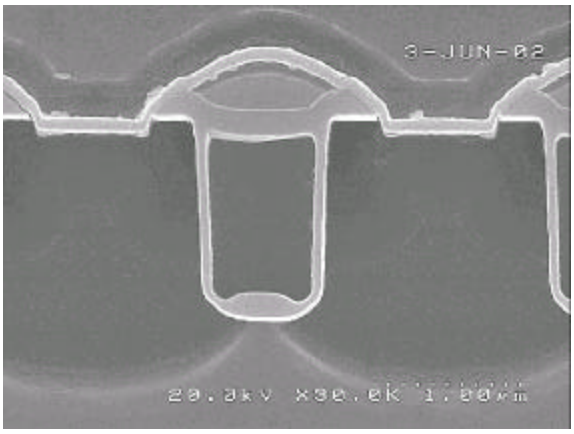

Figure 6. SEM cross-section of a W-Gated Trench MOSFET enlarged cell showing the W-shaped gate.

Measured gate-drain charge of packaged devices was reduced from 3.7 nC to 1.7 nC, as shown in Figure 7, while on-resistance increased from 10 mΩ to 13 mΩ. This corresponds to a 60% reduction in the figure of merit (r_{DSon}*Q_{gd}). Figure 8 shows the significant decrease in C_{rss}, of the WMOSFET when compared with the UMOSFET. At V_{DS}=0 V C_{rss} is reduced from 426 pF to 156 pF.

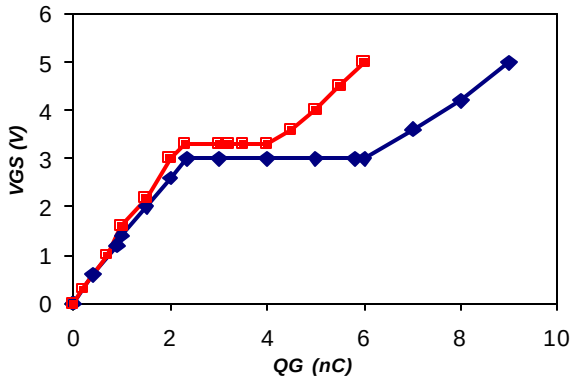

Figure 7. Measured gate charge of a W-gated WMOSFET compared against a conventional Trench UMOSFET.

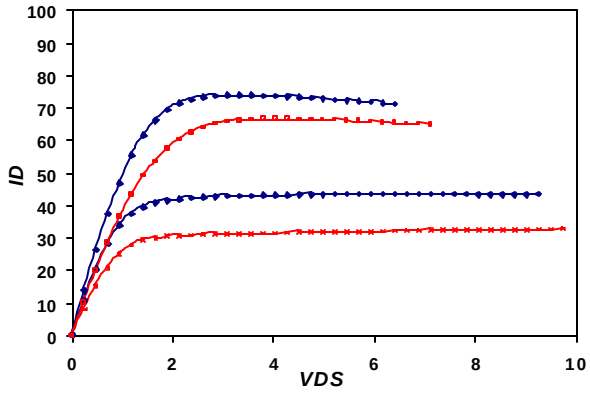

Figure 8. Measured gate drain capacitance (C_{rss}) of a WMOSFET and a conventional UMOSFET.

The first parts to be produced and released by Vishay-Siliconix are given in Table 1. All these have a 30 V V_{ds} rating and a maximum gate voltage of 20 V and are produced in bond wireless SO-8 and PowerPAK SO-8 packages to provide a low inductance package, to aid switching performance.

	$R_{DS(on)}$ max @ V_{gs} [W]		Q_g Typ.	Q_{gs} Typ.	Q_{gd} Typ.
Name	**10 V V_{gs}**	**4.5 V V_{gs}**	**[nC]**	**[nC]**	**[nC]**
Si4390DY	0.0105	0.015	10	7.5	2.1
Si7390DP	0,0105	0.015	10	7.5	2.1
Si4392DY	0.0115	0.0165	10	3.5	2.6
Si7392DP	0.0115	0.0165	10	3.5	2.6

Table 1. Initial 30V V_{ds} and 20V V_{gs} WMOSFET devices to be released.

CONCLUSION

The evolution of fast switching low $r_{DS(on)}$ power MOSFETs has been eagerly anticipated and in recent times Trench Gated structures and ultra high cell density devices have made significant performance improvements. However, the current device technology limits the dynamic of the power MOSFET when operating at high switching frequencies. This paper demonstrated an innovative thick bottom oxide process, which enables C_{rss} to be halved when compared to existing gated structures and thus significantly reduces the gate charge required to turn on the device and also reduces the switching transients of the power MOSFET.

References.

[1] Richard A. Blanchard et al. US patent 4,914,058 April 3, 1990.

[2] R.J.E Hueting , et al. “Switching Performance of low-voltage N-channel Trench MOSFETs” ISPSD Proceedings , June 2002, pp. 177-180

[3] M. Darwish et al. Patents Pending.

[4] Ultra High Cell Density TrenchFET devices: Obtaining that Critical Balance of Switching Performance Verses On Resistance and its Associated Impact on Device Selection. Guy Moxey, PCIM proc. Nuremberg 2002.